



NILASAILA INSTITUTE OF SCIENCE & TECHNOLOGY  
SERGARH-756060, BALASORE (ODISHA)  
(Approved by AICTE& affiliated to SCTE&VT, Odisha)



## LESSON PLAN

**SUBJECT: Th-2 (DIGITAL ELECTRONICS & MICROPROCESSOR)**

### CHAPTER WISE DISTRIBUTION OF PERIODS

Sl.No.	Name of the chapter as per the Syllabus	No. of Periods as per the Syllabus	No. of periods actually needed
1	Basics Of Digital Electronics	15	15
2	Combinational Logic Circuits	15	15
3	Sequential Logic Circuits	15	8
4	8085 Microprocessor	20	20
5	Interfacing And Support Chips	10	10
TOTAL		75	75

Discipline: EEE	Semester: 5 <sup>th</sup>	Name of the Teaching Faculty: Er. RANJAN KUMAR PADHI
Week	Class Day	Theory / Practical Topics
1 <sup>st</sup>	1 <sup>st</sup>	<b>1. BASICS OF DIGITAL ELECTRONICS</b> 1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	2 <sup>nd</sup>	1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system
	3 <sup>rd</sup>	1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system
	4 <sup>th</sup>	1.2 Binary addition, subtraction, Multiplication and Division.
	5 <sup>th</sup>	1.3 1's complement and 2's complement numbers for a binary number
2 <sup>nd</sup>	1 <sup>st</sup>	1.4 Subtraction of binary numbers in 2's complement method.
	2 <sup>nd</sup>	1.5 Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
	3 <sup>rd</sup>	1.6 Importance of parity Bit.
	4 <sup>th</sup>	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	5 <sup>th</sup>	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
3 <sup>rd</sup>	1 <sup>st</sup>	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.
	2 <sup>nd</sup>	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.
	3 <sup>rd</sup>	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression
	4 <sup>th</sup>	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
	5 <sup>th</sup>	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.

4 <sup>th</sup>	1 <sup>st</sup>	<b>2. COMBINATIONAL LOGIC CIRCUITS</b> 2.1 Give the concept of combinational logic circuits.
	2 <sup>nd</sup>	2.2 Half adder circuit and verify its functionality using truth table.
	3 <sup>rd</sup>	2.2 Half adder circuit and verify its functionality using truth table.
	4 <sup>th</sup>	2.3 Realize a Half-adder using NAND gates only and NOR gates only.
	5 <sup>th</sup>	2.4 Full adder circuit and explain its operation with truth table.
5 <sup>th</sup>	1 <sup>st</sup>	2.4 Full adder circuit and explain its operation with truth table.
	2 <sup>nd</sup>	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table
	3 <sup>rd</sup>	2.6 Full subtractor circuit and explain its operation with truth table.
	4 <sup>th</sup>	2.6 Full subtractor circuit and explain its operation with truth table.
	5 <sup>th</sup>	<b>2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer</b>
6 <sup>th</sup>	1 <sup>st</sup>	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	2 <sup>nd</sup>	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	3 <sup>rd</sup>	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	4 <sup>th</sup>	2.9 Working of Two bit magnitude comparator.
	5 <sup>th</sup>	2.9 Working of Two bit magnitude comparator.
7 <sup>th</sup>	1 <sup>st</sup>	<b>3. SEQUENTIAL LOGIC CIRCUITS</b> 3.1 Give the idea of Sequential logic circuits.
	2 <sup>nd</sup>	3.2 State the necessity of clock and give the concept of level clocking and edge triggering,
	3 <sup>rd</sup>	3.3 Clocked SR flip flop with preset and clear inputs.
	4 <sup>th</sup>	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	5 <sup>th</sup>	3.6 Concept of race around condition and study of master slave JK flip flop.
8 <sup>th</sup>	1 <sup>st</sup>	3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	2 <sup>nd</sup>	3.8 Applications of flip flops. 3.9 Define modulus of a counter
	3 <sup>rd</sup>	3.10 4-bit asynchronous counter and its timing diagram.
	4 <sup>th</sup>	3.10 4-bit asynchronous counter and its timing diagram.
	5 <sup>th</sup>	3.11 Asynchronous decade counter.

9 <sup>th</sup>	1 <sup>st</sup>	3.12 4-bit synchronous counter.
	2 <sup>nd</sup>	3.13 Distinguish between synchronous and asynchronous counters.
	3 <sup>rd</sup>	3.14 State the need for a Register and list the four types of registers.
	4 <sup>th</sup>	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
	5 <sup>th</sup>	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
10 <sup>th</sup>	1 <sup>st</sup>	4. 8085 MICROPROCESSOR 4.1 Introduction to Microprocessors, Microcomputers
	2 <sup>nd</sup>	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	3 <sup>rd</sup>	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	4 <sup>th</sup>	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	5 <sup>th</sup>	4.3 Pin diagram and description.
11 <sup>th</sup>	1 <sup>st</sup>	4.3 Pin diagram and description.
	2 <sup>nd</sup>	4.3 Pin diagram and description.
	3 <sup>rd</sup>	4.4 Stack, Stack pointer & stack top
	4 <sup>th</sup>	4.5 Interrupts
	5 <sup>th</sup>	4.6 Opcode & Operand,
12 <sup>th</sup>	1 <sup>st</sup>	4.7 Differentiate between one byte, two byte & three byte instruction with example.
	2 <sup>nd</sup>	4.8 Instruction set of 8085 example
	3 <sup>rd</sup>	4.9 Addressing mode
	4 <sup>th</sup>	4.9 Addressing mode
	5 <sup>th</sup>	4.10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	1 <sup>st</sup>	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write

13 <sup>th</sup>	2 <sup>nd</sup>	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	3 <sup>rd</sup>	4.12 Timing Diagram for 8085 instruction
	4 <sup>th</sup>	4.13 Counter and time delay.
	5 <sup>th</sup>	4. 14 Simple assembly language programming of 8085.
14 <sup>th</sup>	1 <sup>st</sup>	5. INTERFACING AND SUPPORT CHIPS 5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
	2 <sup>nd</sup>	5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
	3 <sup>rd</sup>	5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
	4 <sup>th</sup>	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	5 <sup>th</sup>	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
15 <sup>th</sup>	1 <sup>st</sup>	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	2 <sup>nd</sup>	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	3 <sup>rd</sup>	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	4 <sup>th</sup>	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	5 <sup>th</sup>	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller

Sign. Of HOD

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