



NILASAILA INSTITUTE OF SCIENCE & TECHNOLOGY
SERGARH-756060, BALASORE (ODISHA)
(Approved by AICTE& affiliated to SCTE&VT, Odisha)



LESSON PLAN

SUBJECT: Th-3 (DIGITAL ELECTRONICS & MICROPROCESSOR)

Name Of The Faculty :- Er.Biswajit Parida

Branch :- Electrical Engg.

Session :- 2025-26

Semester :- 5th

Examination :- 2025 (W)

CHAPTER WISE DISTRIBUTION OF PERIODS

Sl.No.	Name of the chapter as per the Syllabus	No. of Periods as per the Syllabus	No. of periods actually needed
1	Basics Of Digital Electronics	15	15
2	Combinational Logic Circuits	15	15
3	Sequential Logic Circuits	15	15
4	8085 Microprocessor	20	20
5	Interfacing And Support Chips	10	10
Total periods		75	75


10/07/2025

Sign of Faculty


10/07/25

Sign of H.O.D.

Name of the programme: Diploma in Electrical Engg.	Semester: 5th	Name of the Teaching Faculty: Er.Biswajit Parida	
		Academic Year : 2025-26	Examination : 2025 (W)
Course Code: (TH-3)	Course Year: Third Year	No. of Classes Alloted Per Week :	5
		Planned Classes Required to Complete the Course	75
Week	Class Day	Topics to be Covered	
1 st	1 st	1. BASICS OF DIGITAL ELECTRONICS 1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system.	
	2 nd	1.2 Binary addition, subtraction, Multiplication and Division.	
	3 rd	1.2 Binary addition, subtraction, Multiplication and Division.	
	4 th	1.3 1's complement and 2's complement numbers for a binary number	
	5 th	1.4 Subtraction of binary numbers in 2's complement method.	
2 nd	1 st	1.5 Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.	
	2 nd	1.6 Importance of parity Bit.	
	3 rd	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.	
	4 th	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.	
	5 th	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.	
3 rd	1 st	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.	
	2 nd	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.	
	3 rd	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.	
	4 th	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression	
	5 th	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.	
4 th	1 st	2. COMBINATIONAL LOGIC CIRCUITS 2.1 Give the concept of combinational logic circuits.	
	2 nd	2.2 Half adder circuit and verify its functionality using truth table.	
	3 rd	2.2 Half adder circuit and verify its functionality using truth table.	
	4 th	2.3 Realize a Half-adder using NAND gates only and NOR gates only.	
	5 th	2.3 Realize a Half-adder using NAND gates only and NOR gates only.	
5 th	1 st	2.4 Full adder circuit and explain its operation with truth table	
	2 nd	2.4 Full adder circuit and explain its operation with truth table	
	3 rd	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table	
	4 th	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table	
	5 th	2.6 Full subtractor circuit and explain its operation with truth table.	

Week	Class Day	Topics to be Covered
6 th	1 st	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	2 nd	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	3 rd	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder
	4 th	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder
	5 th	2.9 Working of Two bit magnitude comparator.
7 th	1 st	3. SEQUENTIAL LOGIC CIRCUITS 3.1 Give the idea of Sequential logic circuits.
	2 nd	3.2 State the necessity of clock and give the concept of level clocking and edge triggering.
	3 rd	3.3 Clocked SR flip flop with preset and clear inputs.
	4 th	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	5 th	3.6 Concept of race around condition and study of master slave JK flip flop.
8 th	1 st	3.6 Concept of race around condition and study of master slave JK flip flop.
	2 nd	3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	3 rd	3.8 Applications of flip flops.
	4 th	3.9 Define modulus of a counter
	5 th	3.10 4-bit asynchronous counter and its timing diagram.
9 th	1 st	3.11 Asynchronous decade counter
	2 nd	3.12 4-bit synchronous counter.
	3 rd	3.13 Distinguish between synchronous and asynchronous counters.
	4 th	3.14 State the need for a Register and list the four types of registers
	5 th	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
10 th	1 st	4. 8085 MICROPROCESSOR 4.1 Introduction to Microprocessors, Microcomputers
	2 nd	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	3 rd	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	4 th	4.3 Pin diagram and description.
	5 th	4.3 Pin diagram and description.
11 th	1 st	4.4 Stack, Stack pointer & stack top
	2 nd	4.5 Interrupts
	3 rd	4.6 Opcode & Operand,
	4 th	4.7 Differentiate between one byte, two byte & three byte instruction with example.
	5 th	4.8 Instruction set of 8085 example

Week	Class Day	Topics to be Covered
12 th	1 st	4.8 Instruction set of 8085 example
	2 nd	4.9 Addressing mode
	3 rd	4 .10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	4 th	4 .10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	5 th	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
13 th	1 st	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	2 nd	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	3 rd	4.12 Timing Diagram for 8085 instruction
	4 th	4.13 Counter and time delay.
	5 th	4. 14 Simple assembly language programming of 8085.
14 th	1 st	5. INTERFACING AND SUPPORT CHIPS 5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
	2 nd	5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
	3 rd	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	4 th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	5 th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
15 th	1 st	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	2 nd	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	3 rd	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	4 th	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	5 th	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller



SIGN. OF FACULTY



SIGN. OF HOD